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## (54) A frequency synthesiser.

(57) A frequency synthesiser comprising a phase locked loop having a reference oscillator coupled to a first input of a comparator, a voltage controlled oscillator (VCO) for providing an output signal, which output signal is fed back by way of a divider circuit for dividing the output fequency by a factor N to a second input of said comparator, the output of the comparator being applied to a control input of the VCO, and including input means for applying a modulating signal in binary format via integrator means for control of the divider circuit, and means having a predetermined transfer function coupling said modulating signal to the control input of the VCO whereby to provide a modulation of the output signal in desired format.

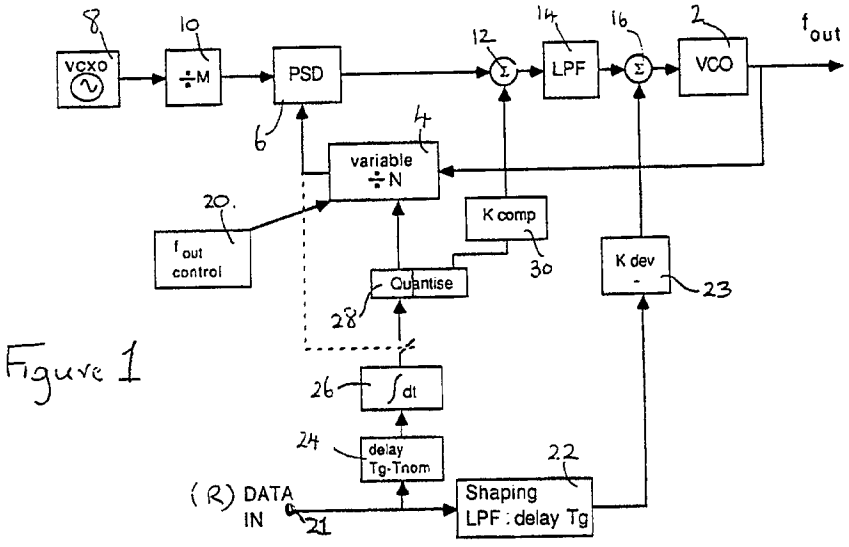


Figure 1

Two Point Modulated Synthesiser With N Counter Modulation
(approximations used for implementation)

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# A FREQUENCY SYNTHESISER

## FIELD OF THE INVENTION

This invention relates to frequency synthesis, in particular direct modulation of a frequency synthesiser to produce wide band modulation. The present invention has particular though not exclusive application to cellular radio, for mobile telephone systems, and especially the GSM (Groupe Speciale Mobile) system.

## BACKGROUND ART

In the GSM system, data to be transmitted is modulated onto a 900 MHz carrier by a Gaussian minimum shift keying technique (GMSK). GMSK is a form of continuous phase frequency shift keying in which the modulating data is subject to a Gaussian low pass filter. Frequency Channels are provided at a spacing of 200 kHz and data is transmitted on each channel at a total rate of 270.833 $kbits^{-1}$.

One major problem is that of modulation of data onto the UHF carrier wave. GMSK modulation produces a lower spectral occupancy than frequency shift keying or differential phase modulation. In GSM, the data transmission rate (270.833 kbit/s) is higher than the channel spacing (200 kHz). The bandwidth of the signal must be less than 200 kHz, and this makes the task of modulation difficult.

Normally a phase lock loop system is employed for frequency synthesis so that the transmission frequency as synthesised by the frequency synthesiser can rapidly be changed between channels by changing the division ratio. Conventional methods of modulation, such as modulating the frequency produced by a crystal and then mixing that signal with a UHF signal poduced from a synthesiser are too bulky and expensive to be employed in say a user hand set of a mobile telephone. Methods have therefore been developed for modulating directly the phase lock loop. One method which is employed for direct modulation is to modulate the phase of a reference crystal oscillator for the phase lock loop. However the problem here is that modulation frequencies are required down to DC and up to around 250 kHz. The high frequency modulations will be filtered out by the filters within the phase lock loop. Another method is direct modulation of the VCO in the phase locked loop. Here however the low frequency modulations are filtered out by the loop.

A method which has been employed to overcome these problems of modulation in phase lock loops is known as two-point modulation schemes.

Two-point modulation schemes have been employed with modulation of the ÷N divider and the control input of the VCO. For example US-A-4,543,542, US-A-4,810,977 and EP-A-0322139 disclose analog FM modulation of a frequency synthesiser in test equipment. The analog modulating signal is applied via an A/D converter to a ÷N divider. GB-A-2046541 discloses direct modulation of a frequency synthesiser by digital (binary level) modulation with the modulating signal applied direct to the ÷N divider and via a D/A converter and low pass filter to a control input of the VCO. In this way, a simple frequency shift keying of the output signal is achieved, for example for a teleprinter.

None of these known arrangements would be suitable for producing continuous phase modulation of a carrier frequency by application of digital modulating signals.

## SUMMARY OF THE INVENTION

It is an object of the present invention to provide an inexpensive means of modulating a frequency synthesiser, suitable for incorporation into a handset of a mobile/portable telephone system, and which desirably produces continuous phase modulated signals from a digital input modulating signal.

The present invention provides a frequency synthesiser comprising a phase locked loop having a reference oscillator coupled to a first input of a comparator, a voltage controlled oscillator (VCO) for providing an input signal, which input signal is fed back by way of a divider circuit for dividing the output frequency by a factor N to a second input of said comparator, the output of the comparator being applied to a control input of the VCO, and including input means for applying a modulating signal in binary format via integrator means for control of the divider circuit, and means having a predetermined transfer function coupling said modulating signal to the control input of the VCO whereby to provide a modulation of the output signal in desired format.

Thus in accordance with the invention, where GMSK modulation is required, the transfer function means provides a Gaussian filter function. Where other forms of continuous phase modulation (CPM) are required, e.g.a raised cosine modulation, an appropriate filter will be provided. For a description and definition of various types of CPM, reference is made to "Digital Phase Modulation" Anderson, Aulin, Sundberg, Plenum Press pp. 50-53. This reference includes a mathematical definition of

CPM, but for present purposes it is sufficient to understand CPM as meaning a constant carrier wave envelope but with phase varying in a continuous manner.

It would be possible in accordance with the invention to provide minimum shift keying (fast frequency shift keying) wherein the modulation waveform usually has a phase quadrature form. It may be produced by providing a direct connection as the transfer function means.

Thus in accordance with the invention if a modulation input signal produces a phase or frequency change in the output of the voltage controlled oscillator, the modulation input signal is arranged to produce a corresponding change in the variable divider value N such that the divided value of frequency applied to the phase sensitive detector remains constant so that the phase sensitive detector does not experience any apparent change of frequency.

Thus, if a change in modulation input signal dR produces a change df in the VCO output signal f, and a change dN in the divider value N, then for a constant frequency value $f_N$ applied to the input of the phase sensitive detector:

$$f_N = \frac{f}{N} = \frac{f + df}{N + dN}$$

$\therefore f(N + dN) = N(f + df)$

$fN + fdN = Nf + df$

thus $\frac{dN}{N} = \frac{df}{f}$ for correction operation.

However in situations where the value of N is low, or the frequency deviations at the VCO output are small then it may not be possible to get sufficient resolution in the incremental value dN to provide appropriate compensation. Thus in accordance with a further feature of the invention an extra compensation signal with finer resolution may be added at an appropriate part of the circuit, for example the loop filter input.

## BRIEF DESCRIPTION OF THE DRAWINGS

A preferred embodiment of the invention will now be described with reference to the accompanying drawings wherein:-

Figure 1 is a block schematic view of a phase lock loop of a freuency synthesiser according to the invention incorporating a two point modulation scheme; and,

Figure 2 is a more detailed block diagram of a frequency synthesiser of Figure 1.

## BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to Figure 1, the synthesiser according to the invention includes a phase locked loop wherein, a VCO 2 provides an output signal $f_{out}$, and this signal is fed back to a variable ÷N circuit 4, then to a phase sensitive detector 6 which compares the divided down frequency with a reference frequency provided by a reference oscillator 8 coupled via a ÷M circuit 10 to a second input of detector 6. The output of the phase detector 6 is provided via a summing circuit 12 to the low pass filter 14 of the loop and then via a further summing circuit 16 to the control input of the VCO 2. Divider circuit 4 has the dividing number N determined via a control circuit 20. An input port 21 is provided for a modulating signal to be applied to the synthesiser. The modulating signal is in any convenient binary format for example NRZ. This binary data signal is applied via a Gaussian filter 22 and a scaling circuit 23 to the summing circuit 16 where the binary data, shaped by filter 22 is applied to the control input of oscillator 2. This therefore is the basic means by which modulation of the output frequency is produced and by employing a Gaussian filter, GMSK modulation is produced. In order to prevent the modulation in the output signal from adversely affecting detector 6, the input data signal is also applied via a delay circuit 24 to an integrator circuit 26 and a quantiser circuit 28. Delay circuit 24 is provided to compensate for the delay introduced by filter 22 relative to the delay in the units 26, 28. Integrator 26 which may be a simple accumulator or counter provides an output signal which is quantised at 28 so that the most significant bit is applied to the variable divider circuit 4 whereas the less significant bits are applied via a scaling circuit 30 to summer circuit 12.

Thus in operation of the invention, when modulation input signal R is applied this produces a signal RKdev which is summed at 16 with the signal from low pass filter 14 to produce a deviation in the output frequency of oscillator 2. In addition this modulation input signal is integrated to produce a phase change signal which is applied to divider N to produce an appropriate change in the value of N. It may be understood that a change in N is equivalent to a phase change in the divided signal $f_N$, since a single cycle of VCO output f when divided by N may be thought of in simple terms as equivalent to a phase change $N^{-1}*2\pi$. This change in the value of N is arranged to cancel out the change in output frequency of oscillator 2 so that the signal applied to phase sensitive detector 6 remains constant. In situations where the absolute value of N is low, it may not be possible to produce a change in N which is sufficiently resolved to achieve appropriate compensation and

in these circumstances the integrated value of phase change applied to via scaling circuit 30 to summing unit 12 produces a further correction in the output from phase sensitive detector 6 to compensate to the required degree of fine resolution.

Referring now to Figure 2 this shows the circuit of Figure 1 in more detail and similar parts are denoted by the same reference numeral. The circuit of Figure 2 is specifically designed for the GSM system and data is input at the prescribed rate of 270.83 kbits per second in unipolar format. A bipolar conversion circuit 40 is coupled between input 21 and Gaussian filter 22.

Counter 4 is of the N/N+1 form in which a latch circuit 20 contains a 13 bit word determining the output frequency, which will be around 900 MHz. The most significant 7 bits of the frequency word are applied to a fixed counter 42. The less significant 6 bits are applied to a swallow counter 44 this provides an output via logic gate 46 to scaler circuit 48 which provides a 64/65 division facility. Counter 44 is clocked by the output of scaler circuit 48 so that when the counter counts to its maximum, the carry output changes to change the scaler circuit 48 from a divide by 64 capability to a divide by 65 capability. In this way counter 44 determines the time prescaler spends in divide by 64 mode relative to divide by 65 mode. This arrangement therefore provides the well known fractional N synthesiser. Scaler circuit 48 is also actuated by logic gate 46 by a control signal from accumulator/quantiser circuits 26/28. Counter circuit 26 is implemented as a M bit up/down counter 50. The output of the counter is applied via a latch circuit 52 and a down counter 54 to scaler circuit 30. The function of down counter 54 is to provide an output pulse having a width proportional to the value stored in latch 52 so that an output pulse is applied to loop 14 having a width proportional to the value in counter 50.

The carry and borrow outputs of counter 50 are applied as the most significant bits of the counter to a latch and logic circuit 58 which provides a 2 bit data output to a modulus counter 60. Counter 60 has a nominal value of 1. This counter is incremented by a 2 bit output from latch circuit 58 and a carry signal from counter 60 is used to enable logic gate 46. Thus it may be seen that the output of the prescaler 44 is modulated by the input data.

Thus in operation, latch 20 (and hence swallow counter 44) is loaded with a number (N-1), i.e one less than the nominal value required for the desired operating frequency of about 900 MHz. The nominal value of 1 in the modulating counter 60 supplies the extra digit required for the nominal operating frequency. Thus in normal operation without any modulating signal applied, swallow counter 44 determines the relative number of cycles that prescaler circuit 48 will divide by 64 and divide by 65. Since MOD counter 60 is clocked by the outputs of counter 44 and prescaler 48, gate 46 is arranged to provide an appropriate pulse signal, whose length is dependant on the value in MOD counter 60(01) to scaler 48, which effectively lengthens the period of time that prescaler 48 is in one count mode. This enables the desired operating frequency to be attained. In the situation where a modulating signal is applied via input 22, the value of counter 60 may change to 2 or 0 depending on the state of latch circuit 58. If the value of counter 60 is 2 then the pulse output of counter 60 is lengthened. This will increase the frequency provided by circuit 4. If however the value of the counter 60 is 0 then no enabling pulse will be provided to prescaler 48 and thus the frequency provided by circuit 4 will be decreased. This method of modulation is acceptable since only fairly small changes in frequency are envisaged (the modulation index = 0.5). This corresponds to a maximum phase change of $\pi/2$ per symbol period.

Thus in summary, in operation of the circuits of Figures 1 and 2, the synthesiser loop is modulated in two points with extra compensation at a third point.

Data is fed through a modulation shaping filter and then applied directly to the VCO. The modulation filter reduces the spectral occupancy of the resulting signal at the VCO output and its shape is dependent on the modulation scheme used, e.g. Gaussian shaping for GMSK.

The modulation on the VCO output is removed before reaching the phase detector, by modulating the N counter. A simple digital approximation to the shaping filter is used to reproduce the modulation (for certain modulation schemes this shaping approximation may be omitted completely whilst still giving an accurate enough representation of the modulation, e.g. GMSK). This approximation to the modulation is integrated digitally (using an up-down counter) and used to modulate the N counter thus removing the modulation on the VCO output.

Due to the fact that N is an integer and is only changed by ±1 on each reference cycle a third point of modulation is required. This removes the phase errors between the quantisation that modulating N imposes (N-1, N, N+1) i.e. phase errors of less that $\pm 2\ \pi$ radians at RF.

The resulting signal is low pass filtered, this removes the high frequency phase errors caused by only using a simple approximation to the modulation shaping when modulating the ÷N counter.

The output of the low pass filter is then the loop error signal with no error due to modulating the VCO and the loop operates as if no modulation had been applied.

## Claims

1. A frequency synthesiser comprising a phase locked loop having a reference oscillator coupled to a first input of a comparator, a voltage controlled oscillator (VCO) for providing an output signal, which output signal is fed back by way of a divider circuit for dividing the output frequency by a factor N to a second input of said comparator, the output of the comparator being applied to a control input of the VCO, and including input means for applying a modulating signal in binary format via integrator means for control of the divider circuit, and means having a predetermined transfer function coupling said modulating signal to the control input of the VCO whereby to provide a modulation of the output signal in desired format.

2. A synthesiser according to Claim 1 wherein the transfer function means is a Gaussian low pass filter in order to produce GMSK modulation.

3. A synthesiser according to Claim 1 wherein the transfer function means is a direct connection for producing MSK modulation.

4. A synthesiser according to any preceding claim wherein the divider circuit includes control means for producing a division factor of N or N+1, and the output of the integrator means is arranged to control the number of cycles of the divider in the N division mode relative to the N+1 division mode.

5. A frequency synthesiser comprising a phase locked loop having a reference oscillator coupled to a first input of a comparator, a VCO for providing an output signal which output signal is fed back by way of a divider circuit for dividing the output frequency by a factor N to a second input of said comparator, the output of the comparator being applied to a control input of the VCO, including input means for applying a modulating signal via integrator means for control of the divider circuit, and the modulating signal being coupled to the control input of the VCO, in order to provide a modulation of the output signal in desired format, wherein the divider circuit includes control means for producing a division factor of N or N+1, and the output of the integrator is arranged to control the number of cycles of the divider in the N mode relative to the N+1 mode.

6. A synthesiser according to Claim 4 or 5 wherein the divider circuit includes a first counter for determining a nominal value of N, a swallow counter for controlling a prescaler circuit, the prescaler circuit being coupled to receive the output of the VCO and to divide the VCO frequency by (n) or (n+1), wherein the swallow counter determines the switching of the prescaler circuit between the (n) and (n+1) modes.

7. A synthesiser according to Claim 6 wherein the integrator means provides a control output for control of the switching of the prescaler circuit.

8. A synthesiser according to Claim 7 wherein the integrator means includes a counter which provides said control output in the form of a pulse whose length is dependant on the value of the counter and which controls the switching of the prescaler circuit.

9. A synthesiser according to any preceding claim wherein the integrator means comprises an up/down counter, the carry/borrow outputs of which are coupled to a further counter means, the output of which is coupled to the divider circuit.

10. A synthesiser as claimed in Claim 9 wherein the value of the up/down counter is applied to a circuit for producing a pulse of variable width, which is applied via scaling means to a summing device for summing with the output of said comparator for compensating for situations where N is small.

11. A synthesiser as claimed in Claim 1 or 5 including summing means for summing an input signal or the output signal of the comparator with a signal derived from the input modulation signal for compensation in situations where N is small.

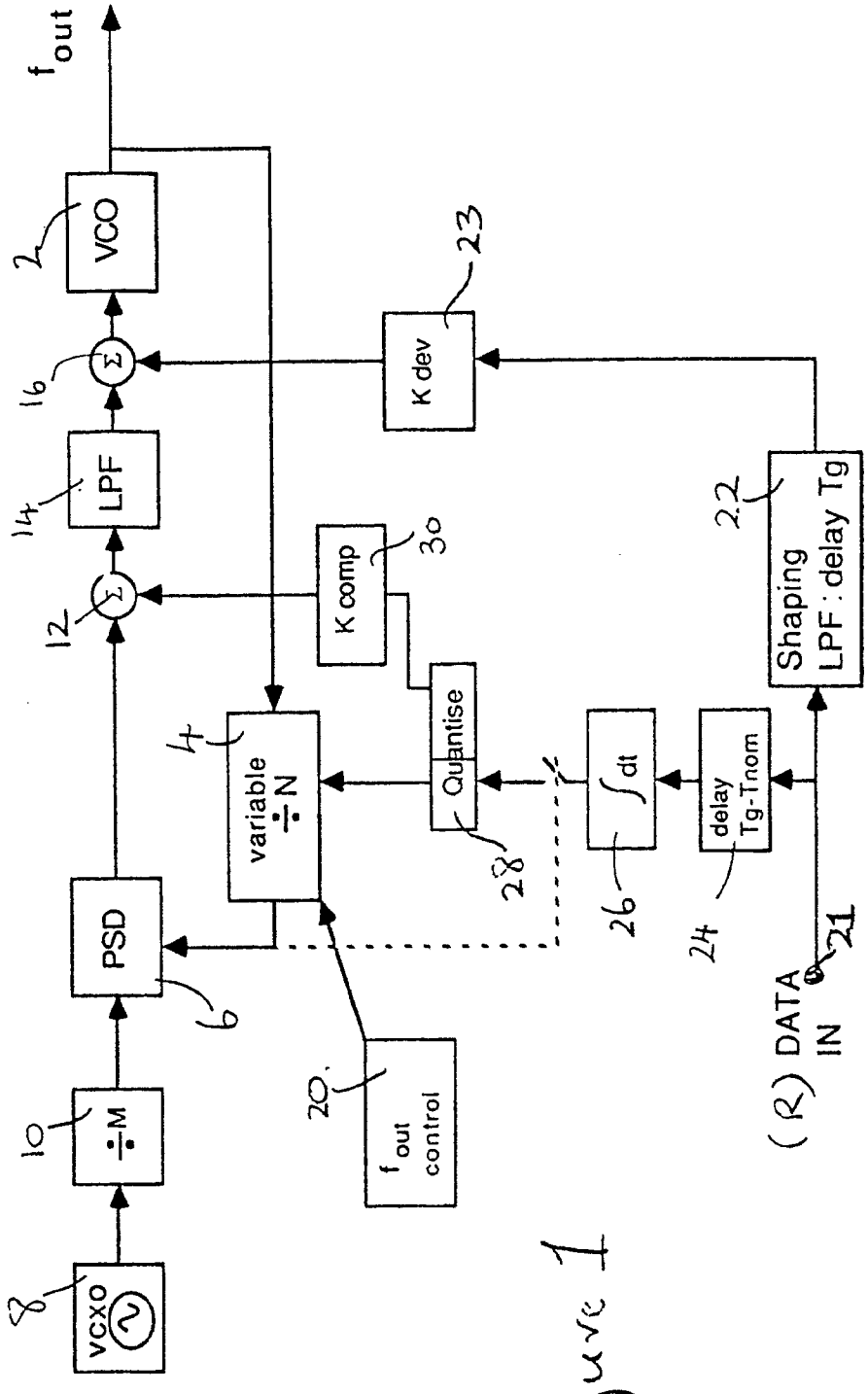


Figure 1

Two Point Modulated Synthesiser With N Counter Modulation (approximations used for implementation)

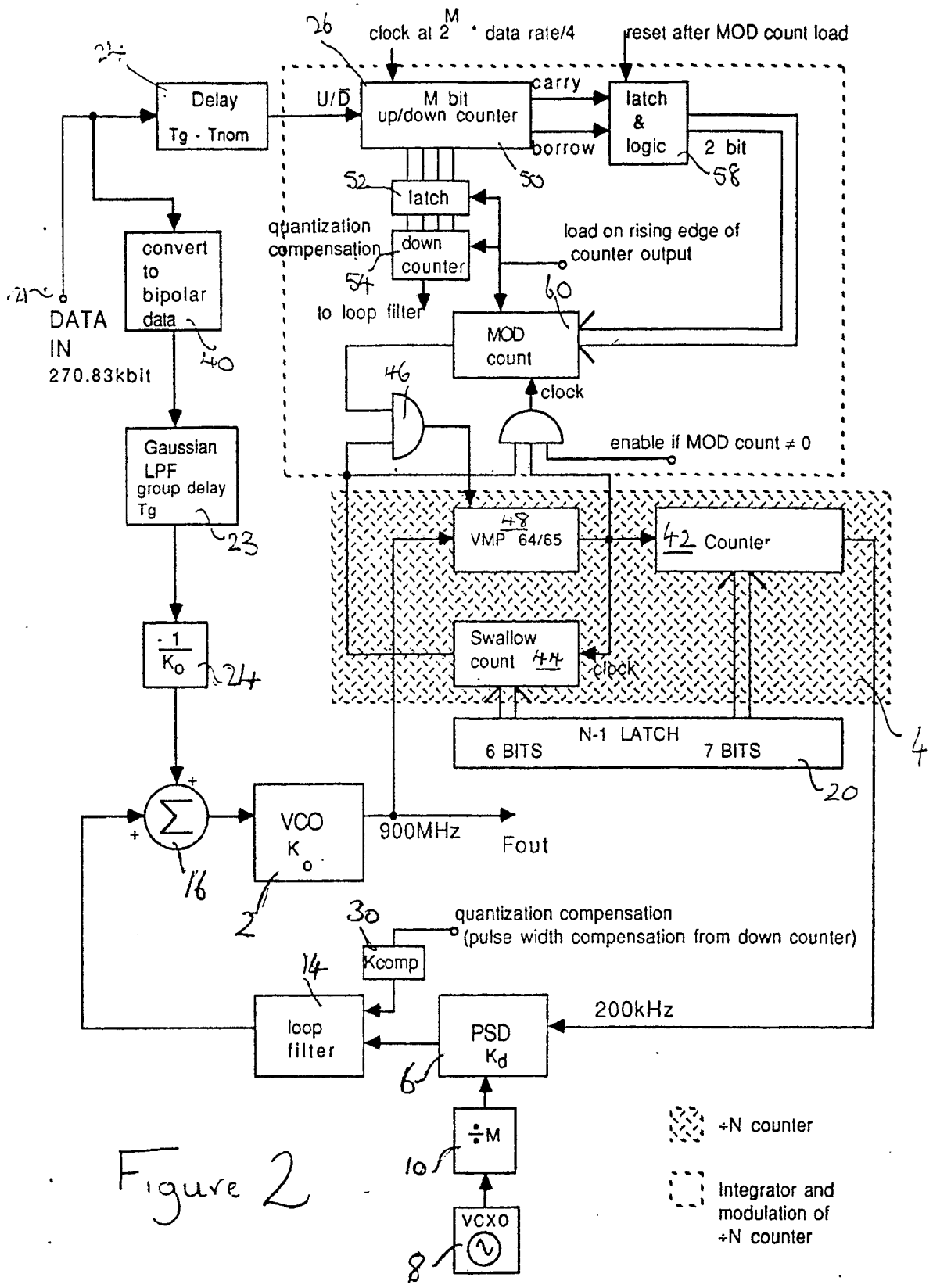


Figure 2

GMSK Modulated synthesiser (VCO & '÷N' modulation)